REMARKS

Applicants respectfully request favorable reconsideration of this application, as amended.

By this Amendment, Claims 1, 10, 11, 14, 18, 28, and 29 have been amended to more particularly recite subject matter which Applicants regard as the invention, as discussed in detail below, as well as to address the alleged informalities therein. The claims have also been amended for consistency and clarity of expression. Claims 12, 13, 15, 16, 21, and 22 have been cancelled without prejudice or disclaimer to reduce the issues, and Claims 19 and 30 have been amended to address the alleged informalities therein.

Thus, Claims 1-11, 14, 17-20, and 23-31 are pending.

The specification has been amended to correct an obvious typographical error in conformance with the drawings.

Turning to the merits, in the Office Action Claims 1-5, 10, 12-15, 18-23, and 28-31 were rejected under 35 U.S.C. § 103 over Ishibashi in combination with Choi; Claims 11-13 and 29-31 were rejected under 35 U.S.C. § 103 over Ishibashi and Choi in further combination with Norton; Claims 6-9 and 24-27 were rejected under 35 U.S.C. § 103 over Ishibashi and Choi in further combination with Yamada; and Claims 16 and 17 were rejected under 35 U.S.C. § 103 over Ishibashi and Choi in further combination with Lee.

Without acceding to the rejections, Claim 1 now recites, *inter alia*, that the first non-volatile memory includes a plurality of switch circuits; a first control signal line; a plurality of first control signal sub-lines; and a second control signal line;

in which the first control signal line is coupled with corresponding first control signal sub-lines via a corresponding switch circuit, said switch circuit constructed to select among various ones of said first control signal sub-lines,

the first control signal sub-line is coupled with the first gate terminals of a predetermined number of the non-volatile memory cells in one row and a corresponding switch circuit, and

the second control signal line is coupled with the second gate terminal of the non-volatile memory cells in one row, and

that the second non-volatile memory includes the first control signal line and the second control signal line, the first control signal line is coupled with the first gate terminal of the non-volatile memory cells in one row, and the second control signal line is coupled with the second gate terminal of the non-volatile memory cells in one row.

Support is provided, for example, at page 23, lines 9-11; page 33, line 7 to page 35, line 20; page 42, lines 15-23; and FIGS. 1, 8, 9, 20, and 34 of Applicants' disclosure.

It is apparent that the applied references do not teach or suggest this combination of features.

For example, the Office Action acknowledges at pages 4-5 that the primary reference, Ishibashi, does not teach or suggest a particular structure of cells. It follows, of course, that Ishibashi cannot teach or suggest Applicants' above-discussed particular structure and arrangement of control signal connections which are different for each of two non-volatile memory cells as recited in Claim 1.

The secondary references are also not seen as teaching or suggesting this combination of features. For example, secondary reference Choi is directed to a flash memory cell that includes a program/erasure gate (35) formed on an oxide-nitride-oxide (ONO) layer (34), and a selecting gate (37). *See* Choi, col. 3, lines 12-43; and FIG. 3. However, it is apparent that Choi does not teach or suggest that a first non-volatile memory includes a plurality of switch circuits; a first control signal line; a plurality of first control signal sub-lines; and a second control signal line;

in which the first control signal line is coupled with corresponding first control signal sub-lines via a corresponding switch circuit, said switch circuit

constructed to select among various ones of said first control signal sub-lines,

the first control signal sub-line is coupled with the first gate terminals of a predetermined number of the non-volatile memory cells in one row and a corresponding switch circuit, and

the second control signal line is coupled with the second gate terminal of the non-volatile memory cells in one row, and

that the second non-volatile memory includes the first control signal line and the second control signal line, the first control signal line is coupled with the first gate terminal of the non-volatile memory cells in one row, and the second control signal line is coupled with the second gate terminal of the non-volatile memory cells in one row, as recited in Claim 1.

Furthermore, secondary reference Yamada teaches a volatile memory, RAM (10), and a non-volatile memory, ROM (11), connected to a common decoder (12) by a common word select line. *See* Yamada, Abstract.

In addition, the cited portion of secondary reference Lee teaches a word line driver (661) connected to a number of word line latches (67a-67h) via corresponding decoders (663a-663h) and a multiplexer (662). *See* Lee, col. 24, lines 30-45; and FIG. 21.

However, neither Yamada nor Lee is seen as remedying the above-noted deficiencies of Ishibashi and Choi. Secondary reference Norton is also not seen as teaching or suggesting this combination of features.

Therefore, Applicants respectfully submit that Claim 1 distinguishes patentably from the applied references.

Furthermore, Claims 10, 11, 14, 18, 28, and 29 also recite that the first non-volatile memory includes a plurality of switch circuits; a first control signal line; a plurality of first control signal sub-lines; and a second control signal line;

in which the first control signal line is coupled with corresponding first control signal sub-lines via a corresponding switch circuit, said switch circuit constructed to select among various ones of said first control signal sub-lines,

the first control signal sub-line is coupled with the first gate terminals of a predetermined number of the non-volatile memory cells in one row and a corresponding switch circuit, and

the second control signal line is coupled with the second gate terminal of the non-volatile memory cells in one row, and

that the second non-volatile memory includes the first control signal line and the second control signal line, the first control signal line is coupled with the first gate terminal of the non-volatile memory cells in one row, and the second control signal line is coupled with the second gate terminal of the non-volatile memory cells in one row.

Therefore, Applicants respectfully submit that Claims 10, 11, 14, 18, 28, and 29 also distinguish patentably for at least the same reasons as discussed above with respect to Claim 1.

Dependent Claims 2-9, 17, 19, 20, 23-27, 30, and 31 are also believed to be patentable due at least to their respective dependence from Claims 1, 14, 18, and 29, respectively, as well as for the additional subject matter recited in Claims 2-9, 17, 19, 20, 23-27, 30, and 31.

Accordingly, a Notice of Allowance is respectfully requested.

The Commissioner is hereby authorized to charge to Deposit Account No. 50-1165 (XA-10261) any fees that may be required by this paper and to credit any overpayment to that Account. If any extension of time is required in connection with the filing of this paper and has not been requested separately, such extension is hereby requested.

Respectfully submitted,

September 3, 2010

By: /Eric G. King/
Mitchell W. Shapiro
Reg. No. 31,568

Eric G. King
Reg. No. 42,736

Miles & Stockbridge P.C.
1751 Pinnacle Drive, Suite 500
McLean, Virginia 22102-3833
(703) 903-9000

MWS:EGK